Data Sheet For 8251 Serial Control Unit

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	24th Dec '11	Initial Version	NU
REL 1.0	16th Aug '12	Removed implementation results	VC

Table of Contents

List Of Figures

List Of Tables

1 Introduction

1.1 Purpose

This document describes the Technical Specification 8251 serial control unit. It includes the overall features, detailed description, I/O specifications and resource utilization summary for the 8251 serial control unit.

1.2 Features

The following features are supported in the Serial Control Unit

- RS-232-C protocol support
- Asynchronous communication only
- Serial interrupt support
- Clock rates of baud rate x 16 or baud rate x 64.
- Character length of 7 or 8 bits
- 1 or 2 Stop bits
- Break transmission
- Automatic break detection
- Full duplex double buffer system
- Parity addition/checking
- Error detection for parity, overrun and framing

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
SCU	Serial Control Unit
DCE	Data Communication Equipment
UART	Universal Asynchronous Receiver Transmitter
DTR	Data Terminal Ready
DSR	Data Set Ready
RTS	Request To Send
CTS	Clear To Send
USART	Universal Synchronous Asynchronous Receiver Transmitter

2 8251 Serial Control Unit

2.1 Block Diagram

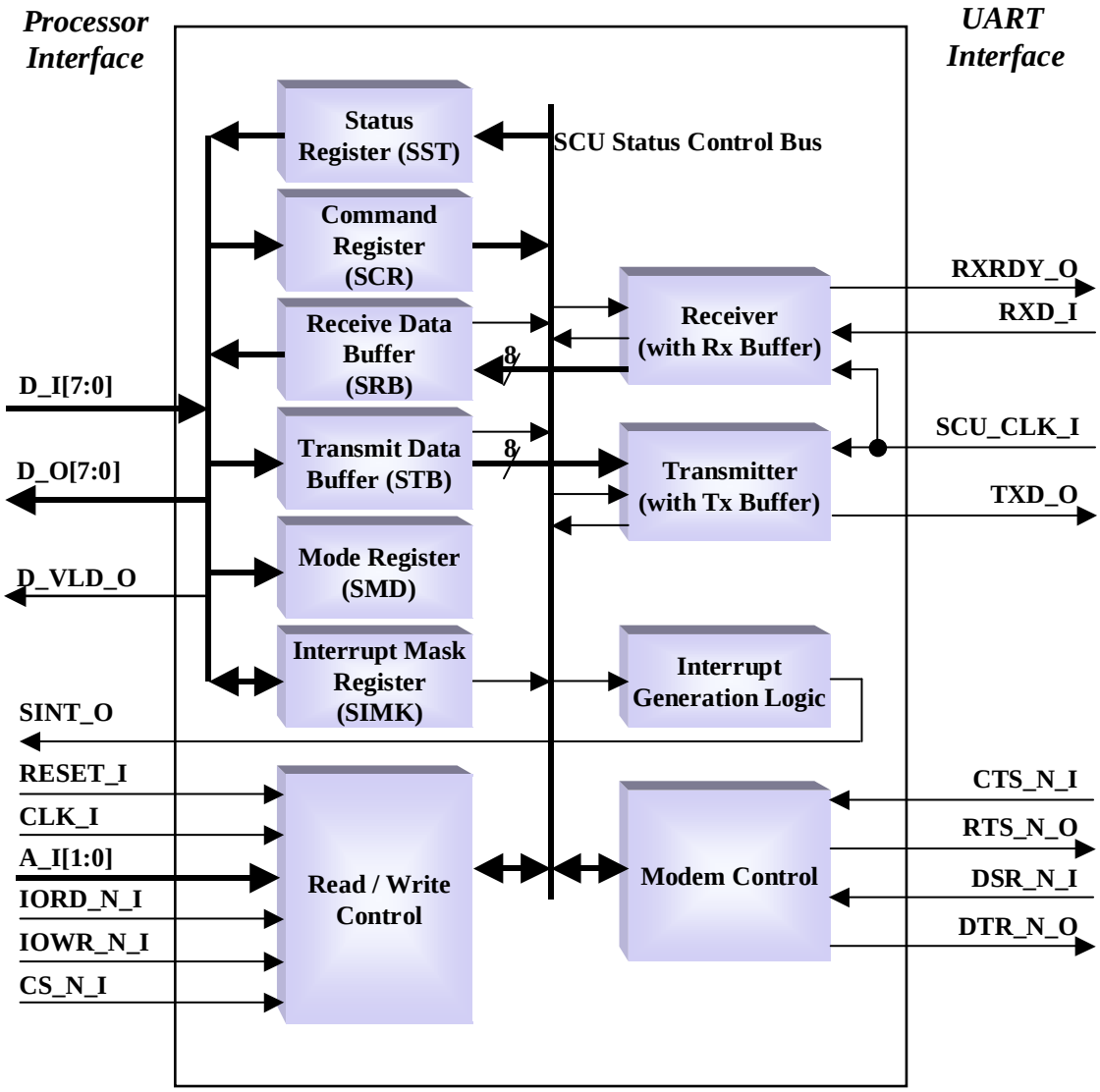

Figure 1: 8251vSerial Controller Block Diagram

2.2 Description

The Serial Controller Unit is an USART based on 8251 with support for asynchronous communication only. The processor can access the unit through I/O read and write commands. The SCU converts parallel data from the processor to serial data and transmit it and convert the serial received data into parallel data for the processor to read. The start bit, parity bit and the stop bits are automatically added in the transmit direction and is stripped in the receive direction.

The design consists of the following main blocks:

- **Read/Write control logic:** This block interfaces with the processor and generates read / write enable signals to the internal registers.
- **Register block:** This block contains all the registers accessible from the processor. These registers control the functionality of the SCU and also provide status of different functions of the SCU to the processor.
- **Interrupt Generation Logic:** This block generates the interrupt to the processor
- **Transmitter:** It also includes a transmit buffer which stores the data from the processor before transmission. This block converts the parallel data to serial data, includes the start, stop and the parity bits before transmitting on the TXD.
- **Receiver:** This block includes the receive buffer which buffers the incoming data from the RXD. This block detects the valid incoming data, strips the start, stop and parity bits, converts it into parallel data before storing in the receive buffer for the processor to read.
- **Modem control:** This block generates the modem interface signals like RTS_N and DTR_N. The RTS_N, CTS_N, DSR_N and DTR_N can also be used as general-purpose I/O pins.

2.3 I/O Signal Description

2.3.1 Processor Interface Signal Description

Table 2: Processor Interface Signal Description

SIGNAL	I/O	WIDTH	DESCRIPTION
RESET_I	I	1	Active high asynchronous reset signal
CLK_I	I	1	Processor Clock signal
IORD_N_I	I	1	Active low IO Read signal from the processor. This signal is active low when reading data or status information or interrupt mask information from the core
IOWR_N_I	I	1	Active low IO Write signal from the processor. This signal is active low when writing data or mode byte or command byte or interrupt mask information to the core
CS_N_I	I	1	Active low Chip select signal from the processor
D_I[7:0]	I	8	Data from the Processor to the Core
D_O[7:0]	O	8	Data from the core to the processor
D_VLD_O	O	8	Active high data valid Signal which indicates the valid data on the data bus from the core to processor
A_I[1:0]	I	2	Processor address bits A[1:0] or A[2:1] for register address decoding
SINT_O	O	1	Active high Serial interrupt from the core towards processor

2.3.2 USART Interface Signal Description

Table 3: USART Interface Signal Description

SIGNAL	I/O	WIDTH	DESCRIPTION
SCU_CLK_I	I	1	External clock signal for Transmitter and Receiver
RXD_I	I	1	Receive data (serial)
TXD_O	O	1	Transmit data (serial)

CTS_N_I	I	1	Active low Clear To Send signal. When this signal is asserted, core can transmit the data
RTS_N_O	O	1	Active low Request To Send signal. This signal will be asserted, when core is ready to transmit the serial data.
DTR_N_O	O	1	Active low Data Terminal Ready signal. This signal is asserted, when core is ready to transmit or receive the serial data
DSR_N_I	I	1	Active low Data Set Ready input Signal. Asserted signal indicates that DCE is connected to the telecommunication line
RXRDY_O	O	1	Active high Receive data ready signal from the core. When this signal is asserted, receive data buffer has a valid received data

3 Timing Waveforms

3.1 Processor Cycle

3.1.1 Read Cycle

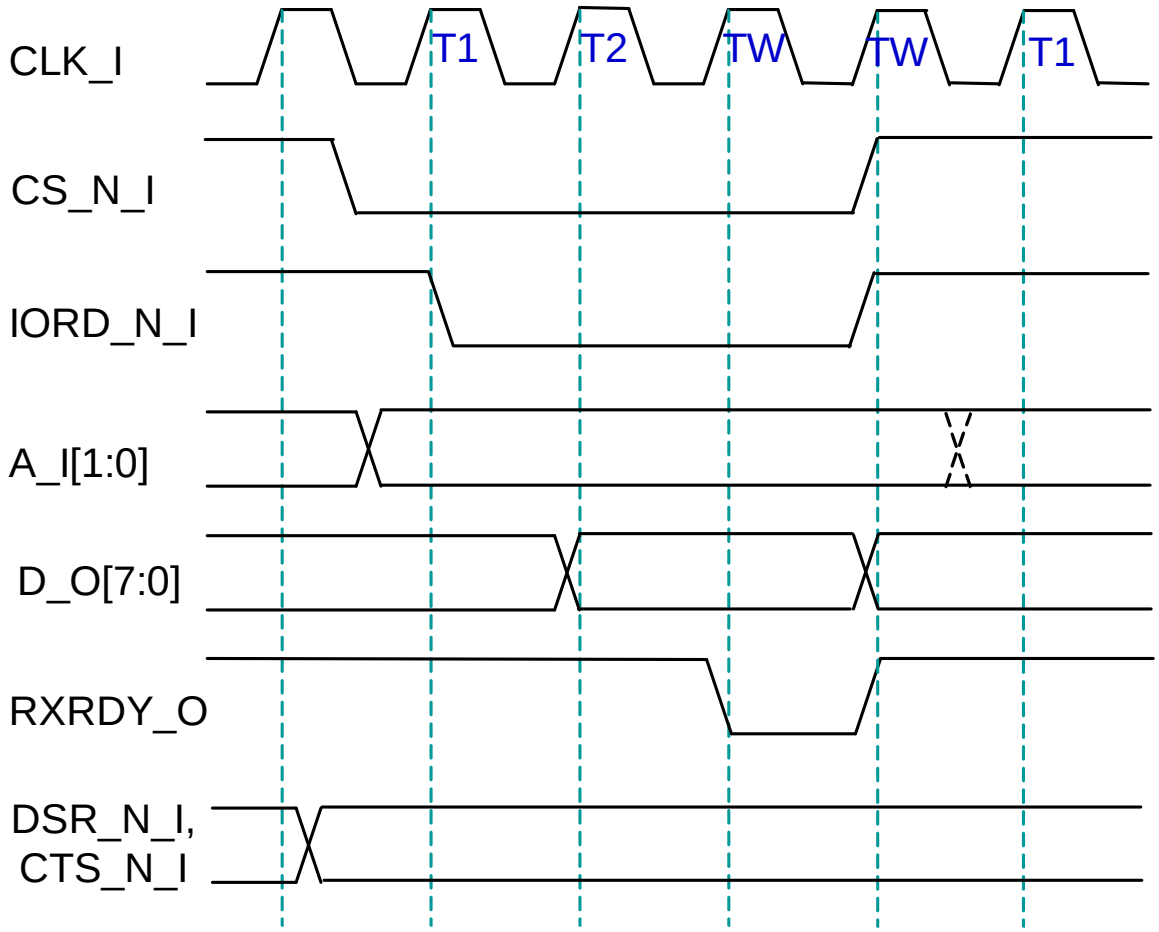

Figure 2: Processor Read Cycle Waveform

3.1.2 Write Cycle

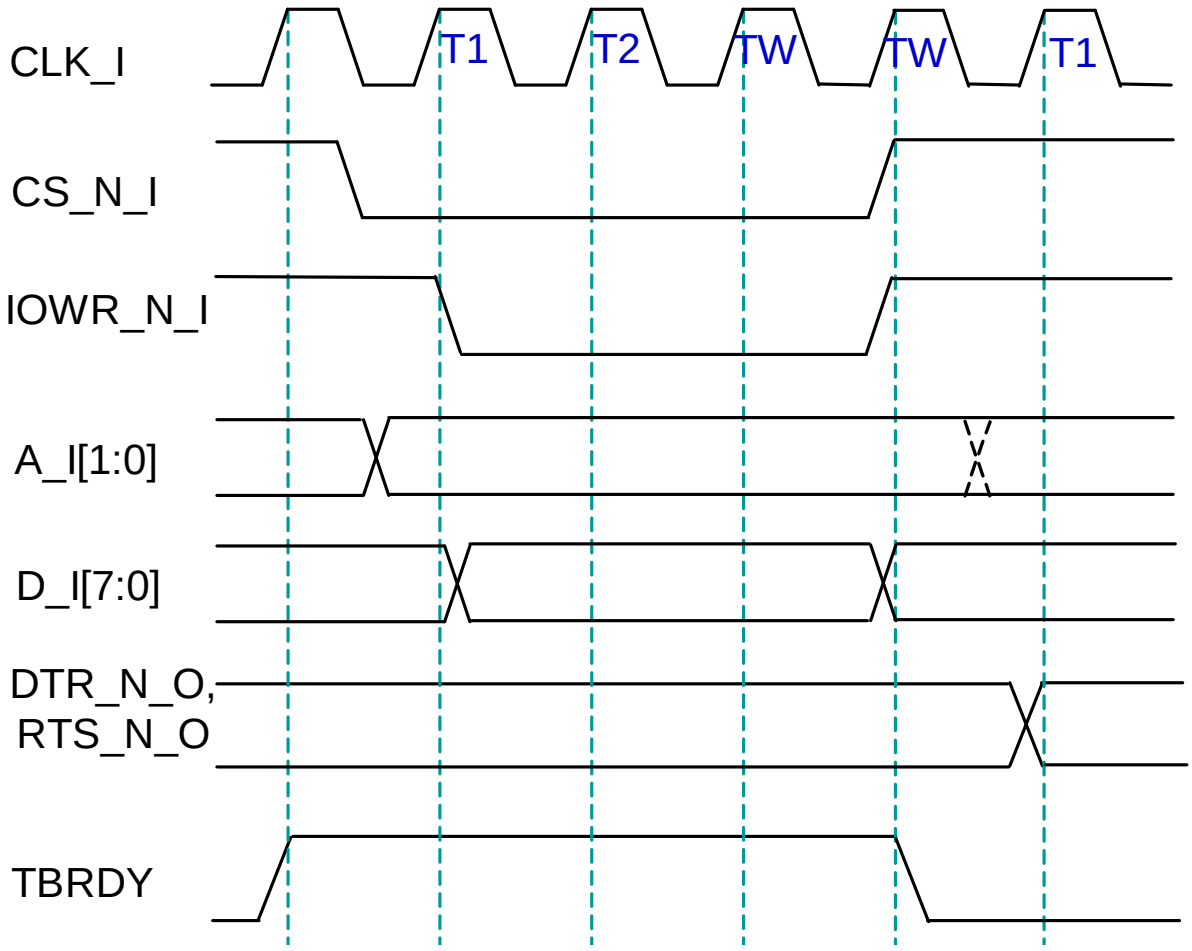

Figure 3: Processor Write Cycle Waveform

3.2 USART Interface waveforms

3.2.1 Transmitter Clock and Tx DATA

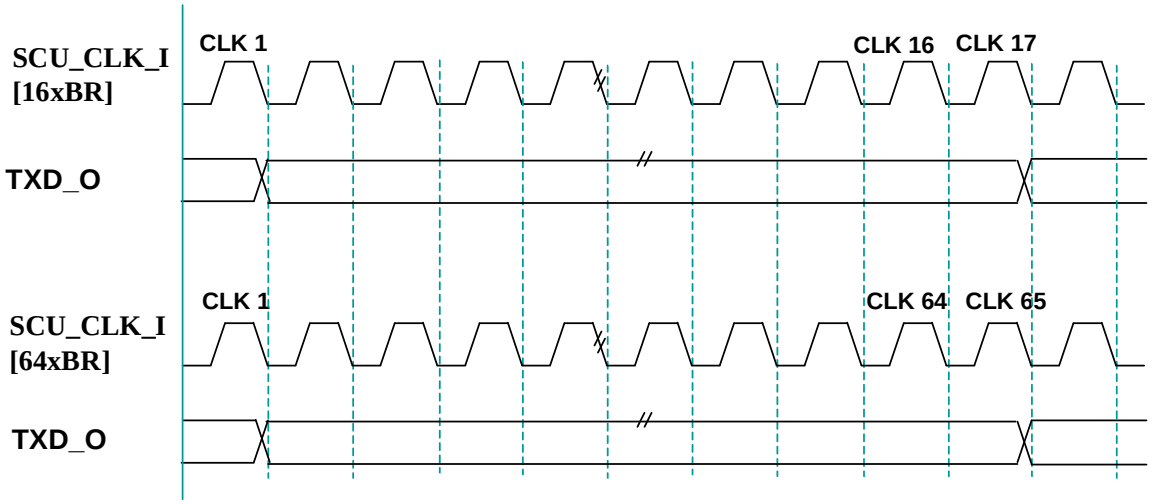

Figure 4: Transmitter Clock and Transmitter data waveform

3.2.2 Receiver Clock and Rx DATA

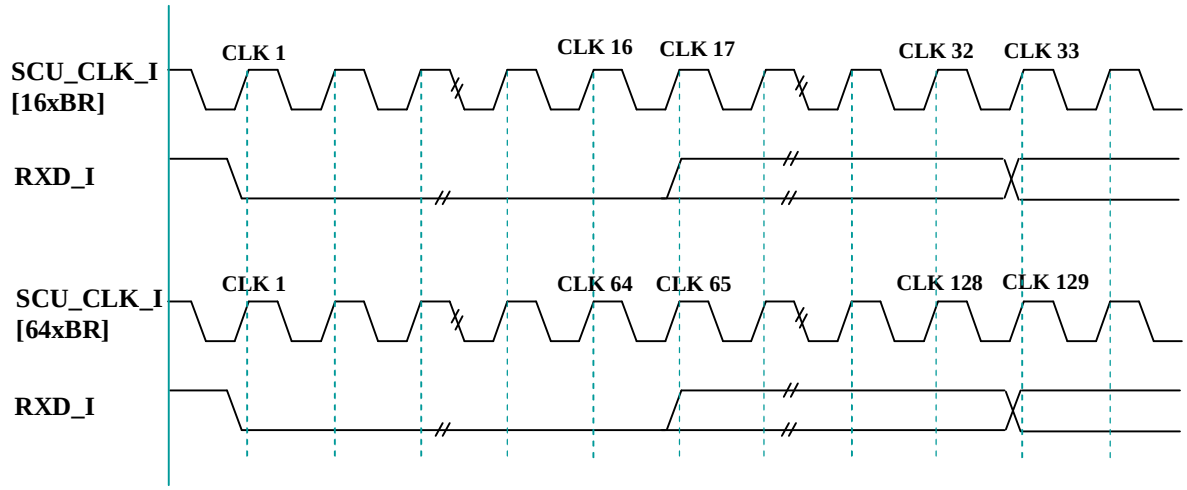

Figure 5: Receiver Clock and Receiver data waveform